AMENDMENTS TO THE SPECIFICATION

The abstract of the disclosure is amended to fit the proper format. Please replace **Abstract** with the following one.

Abstract

An ESD protection circuit is connected to an I/O buffering pad, an internal circuit, a Vss power terminal and a Vdd power terminal. The ESD protection circuit comprises a first ESD-detection circuit, a second ESD-detection circuit, a P-STSCR and an N-STSCR. When a positive-to-Vss ESD event occurs on the I/O buffering pad, the first ESD-detection circuit generates a first trigger current to the P-trigger node of the P-STSCR to trigger the first lateral SCR. The P-STSCR is quickly turned on, and current incurred from the positive voltage pulse is discharged to the Vss power terminal. When a negative-to-Vdd ESD event occurs on the I/O buffering pad, the second ESD-detection circuit generates a second trigger current to the N-trigger node of the N-STSCR to trigger the second lateral SCR. The N-STSCR is quickly turned on, and current incurred from the negative voltage pulse is discharged to the Vdd power terminal.